C. CPU INSTRUCTION ADDRESSING MODES

This appendix describes the addressing modes for the CPU instructions. The following attributes are provided for each addressing mode:

One number of bytes and execution time in clock cycles.

The instructions using the addressing mode.

The format of the instruction.

The instruction operation by clock cycle.

The instruction formats are:

Addressing Mode	No. Bytes	Op Code	Operand	Operand Description
Absolute	3	XXX	nn	nn = 2-byte absolute address
Absolute,X	3	XXX	nn	nn = 2-byte absolute address
Absolute,Y	3	XXX	nn	nn = 2-byte absolute address
Accumulator	1	XXX		
Bit/FF Page (JSB)	1	XXX	b	b = bit 0 –7
Bit/Zero Page (BBR/BBS)	3	XXX	b,n,r	b = bit 0–7, n = 1-byte zero page address, r = 1-byte relative offset
Bit/Zero Page (RMB/SMB)	2	XXX	b,n	b = bit 0–7, n = 1-byte zero page address
Bit/Absolute (RBA/SBA)	4	XXX	bm,nn	bm = byte mask, nn = 2-byte absolute address
Bit/Absolute (BAR/BAS)	5	XXX	nn,bm,rb	bm = byte mask, nn = 2-byte absolute address, r = 1-byte relative offset
Immediate	2	XXX	#n	n = 1-byte constant
Implied	1	XXX		
Indirect Absolute	3	XXX	(nn)	nn = 2-byte absolute address
(Indirect)	2	XXX	(n)	n = 1-byte zero page address of addrLH
(Indirect),X	2	XXX	(n),X	n = 1-byte zero page address of addrLH
Relative	2	XXX	r	r = 1-byte relative offset
Zero Page	2	XXX	n	n = 1-byte zero page address
Zero Page ,X	2	XXX	n,X	n = 1-byte zero page address
Zero Page ,Y	2	XXX	n,Y	n = 1-byte zero page address

C1 IMPLIED ADDRESSING

C1.1 General – 1 Byte, 2 Cycles

Instructions: CLC, CLD, CLI, CLW, CLV, DEX, DEY, INX, INY, NOP, RND, SEC, SED, SEI, TAW, TAX, TAY, TIP, TSX, TWA, TXA, TXS, and TYA

Format: XXX

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	Next OP CODE	Fetch Data (Ignored)	Interpret OP CODE
3	2201	Next OP CODE	Fetch Next OP CODE	Execute instruction, Increment PC to 2202

C1.2 Multiply – 1 Byte, 6 Cycles

Instruction: MPA and MPY

Format: XXX

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	Next OP CODE	Fetch Data (Ignored)	Interpret OP CODE
3	2201	Next OP CODE	Fetch Data (Ignored)	Execute multiply steps
4	2201	Next OP CODE	Fetch Data (Ignored)	
5	2201	Next OP CODE	Fetch Data (Ignored)	
6	2201	Next OP CODE	Fetch Data (Ignored)	
7	2201	Next OP CODE	Fetch Next OP CODE	Finish instruction, Increment PC to 2202

C2 IMMEDIATE ADDRESSING

C2.1 Read – 2 Bytes, 2 Cycles

Instructions: ADC, ADD, AND, CMP, CPX, CPY, EOR, LDA, LDX, LDY, ORA, and SBC

Format: XXX #n n= 1-byte constant

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	Fetch Data	Data	Increment PC to 2202
3	2202	Next OP CODE	Fetch Next OP CODE	Execute instruction, Increment PC to 2203

C2.2 Write – 2 Bytes, 4 Cycles

Instruction: STI

Format: XXX #n n= 1-byte constant

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	Fetch Data	Data	Increment PC to 2202
3	2202	Fetch ADL	ADL	Increment PC to 2203
4	00, ADL	Data	Write Data	Hold PC
5	2203	Next OP CODE	Fetch Next OP CODE	Finish instruction, Increment PC to 2204

C3 ZERO PAGE ADDRESSING

C3.1 Read – 2 Bytes, 3 Cycles

Instructions: ADC, ADD, AND, BIT, CMP, CPX, CPY, EOR, LDA, LDX, LDY, ORA, and SBC

Format: XXX n n = zero page address

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	ADL	Fetch ADL	Interpret OP CODE, Increment PC to 2202
3	00, ADL	Data	Fetch Data	Hold PC
4	2202	Next OP CODE	Fetch Next OP CODE	Finish instruction, Increment PC to 2203

C3.2 Write – 2 Bytes, 3 Cycles

Instructions: STA, STX, and STY.

Format: XXX n n = zero page address

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	ADL	Fetch ADL	Interpret OP CODE, Increment PC to 2202
3	00, ADL	Data	Write Data	Hold PC
4	2202	Next OP CODE	Fetch Next OP CODE	Finish instruction, Increment PC to 2203

C4 ZERO PAGE,X ADDRESSING

C4.1 Read – 2 Bytes, 4 Cycles

Instructions: ADC, ADD, AND, CMP, EOR, LDA, LDY, ORA, and SBC

Format: XXX n,X n = 1-byte zero page address

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	BAL	Fetch BAL	Interpret OP CODE, Increment PC to 2202
3	00, BAL	Data (Ignored)	Fetch Data (Ignored)	Add BAL+X, Hold PC
4	00, BAL+X	Data	Fetch Data	Hold PC
5	2202	Next OP CODE	Fetch Next OP CODE	Finish instruction, Increment PC to 2203

C4.2 Write – 2 Bytes, 4 Cycles

Instructions: STA and STY

Format: XXX n,X n = 1-byte zero page address

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	BAL	Fetch BAL	Interpret OP CODE, Increment PC to 2202
3	00, BAL	Data (Ignored)	Fetch Data (Ignored)	Add BAL+X, Hold PC
4	00, BAL+X	Data	Write Data	Hold PC
5	2202	Next OP CODE	Fetch Next OP CODE	Finish instruction, Increment PC to 2203

C4.3 Write – 2 Bytes, 5 Cycles

Instructions: EXC

Format: XXX n,X n = 1-byte zero page address

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	BAL	Fetch BAL	Interpret OP CODE, Increment PC to 2202
3	00, BAL	Data (Ignored)	Fetch Data (Ignored)	Add BAL+X, Hold PC
4	00, BAL+X	Data	Fetch Data	Hold PC
5	00, BAL+X	Data	Write Data	Hold PC
6	2202	Next OP CODE	Fetch Next OP CODE	Finish instruction, Increment PC to 2203

C5 ZERO PAGE,Y ADDRESSING

C5.1 Read – 2 Bytes, 4 Cycles

Instruction: LDX

Format: XXX n,Y n = 1-byte zero page address

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	BAL	Fetch BAL	Interpret OP CODE, Increment PC to 2202
3	00, BAL	Data (Ignored)	Fetch Data (Ignored)	Add BAL+Y, Hold PC
4	00, BAL+Y	Data	Fetch Data	Hold PC
5	2202	Next OP CODE	Fetch Next OP CODE	Finish instruction, Increment PC to 2203

C5.2 Write – 2 Bytes, 4 Cycles

Instruction: STX

Format: XXX n,Y n = 1-byte zero page address

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	BAL	Fetch BAL	Interpret OP CODE, Increment PC to 2202
3	00, BAL	Data (Ignored)	Fetch Data (Ignored)	Add BAL+Y, Hold PC
4	00, BAL+Y	Data	Write Data	Hold PC
5	2202	Next OP CODE	Fetch Next OP CODE	Finish Instruction, Increment PC to 2203

C6 ABSOLUTE ADDRESSING

C6.1 Read – 3 Bytes, 4 Cycles

Instructions: ADC, AND, BIT, CMP, CPX, CPY, EOR, LDA, LDX, LDY, ORA, and SBC

Format: XXX nn nn = 2-byte absolute address

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	ADL	Fetch ADL	Interpret OP CODE, Increment PC to 2202
3	2202	ADH	Fetch ADH	Hold ADL, Increment PC to 2203
4	ADH, ADL	Data	Fetch Data	Hold PC
5	2203	Next OP CODE	Fetch Next OP CODE	Finish instruction, Increment PC to 2203

C6.2 Write – 3 Bytes, 4 Cycles

Instructions: STA, STX, and STY

Format: XXX nn nn = 2-byte absolute address

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	ADL	Fetch ADL	Interpret OP CODE, Increment PC to 2202
3	2202	ADH	Fetch ADH	Hold ADL, Increment PC to 2203
4	ADH, ADL	Data	Write Data	Hold PC
5	2203	Next OP CODE	Fetch Next OP CODE	Finish Instruction, Increment PC to 2203

C7 ABSOLUTE,X ADDRESSING

C7.1 Read

Instructions: ADC, AND, CMP, EOR, LDA, LDY, ORA, and SBC

Format: XXX nn,X nn = 2-byte absolute address

C7.1a No Page Crossing – 3 Bytes, 4 Cycles

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	BAL	Fetch BAL	Interpret OP CODE, Increment PC to 2202
3	2202	BAH	Fetch BAH	Add BAH+X, Increment PC to 2203
4	BAH, BAL+X	Data	Fetch Data	Hold PC
5	2203	Next OP CODE	Fetch Next OP CODE	Finish instruction, Increment PC to 2204

C7.1b Page Crossing – 3 Bytes, 5 Cycles

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	BAL	Fetch BAL	Interpret OP CODE, Increment PC to 2202
3	2202	BAH	Fetch BAH	Add BAL+X, Increment PC to 2203
4	BAH, BAL+X	Data (Ignored)	Fetch Data (Ignored)	Add BAH+Carry (1), Hold PC
5	BAH+C, BAL+X	Data	Fetch Data	Hold PC
6	2203	Next OP CODE	Fetch Next OP CODE	Finish instruction Increment PC to 2204

C7.2 Write – 3 Bytes, 5 Cycles

Instruction: STA

Format: XXX nn,X nn = 2-byte absolute address

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	BAL	Fetch BAL	Interpret OP CODE, Increment PC to 2202
3	2202	BAH	Fetch BAH	Add BAL+X, Increment PC to 2203
4	BAH, BAL+X	Data (Ignored)	Fetch Data (Ignored)	Add BAH+Carry (0 or 1), Hold PC
5	BAH+C, BAL+X	Data	Write Data	Hold PC
6	2203	Next OP CODE	Fetch Next OP CODE	Finish instruction, Increment PC to 2204

C8 ABSOLUTE,Y ADDRESSING

C8.1 Read

Instructions: ADC, AND, CMP, EOR, LDA, LDX, ORA, and SBC

Format: XXX nn,Y nn = 2-byte absolute address

C8.1a No Page Crossing – 3 Bytes, 4 Cycles

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	BAL	Fetch BAL	Interpret OP CODE, Increment PC to 2202,
3	2202	BAH	Fetch BAH	Add BAL+Y, Increment PC to 2203
4	BAH, BAL+Y	Data	Data	Hold PC
5	2203	Next OP CODE	Fetch Next OP CODE	Finish instruction, Increment PC to 2204

C8.1b Page Crossing – 3 Bytes, 5 Cycles

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	BAL	Fetch BAL	Interpret OP CODE, Increment PC to 2202
3	2202	BAH	Fetch BAH	Add BAL+Y, Increment PC to 2203
4	BAH, BAL+Y	Data (Ignored)	Fetch Data (Ignored)	Add BAH+Carry (1), Hold PC
5	BAH+C, BAL+Y	Data	Fetch Data	Hold PC
6	2203	Next OP CODE	Fetch Next OP CODE	Finish instruction, Increment PC to 2204

C8.2 Write – 3 Bytes, 5 Cycles

Instruction: STA

Format: XXX nn,Y nn = 2-byte absolute address

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	BAL	Fetch BAL	Interpret OP CODE, Increment PC to 2202
3	2202	BAH	Fetch BAH	Add BAL+Y, Increment PC to 2203
4	BAH, BAL+Y	Data (Ignored)	Fetch Data (Ignored)	Add BAH+Carry (0 or 1), Hold PC
5	BAH+C, BAL+Y	Data	Write Data	Hold PC
6	2203	Next OP CODE	Fetch Next OP CODE	Finish instruction, Increment PC to 2204

C9 INDIRECT ADDRESSING

C9.1 Read - 2 Bytes, 5 Cycles

Instructions: ADC, AND, CMP, EOR, LDA, ORA, and SBC

Format: XXX (n) n = Zero page address of absolute address

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	IAL	Fetch IAL	Interpret OP CODE, Increment PC to 2202
3	00, IAL	BAL	Fetch BAL	Add 1 to IAL, Hold PC
4	00, IAL+1	BAH	Fetch BAH	Hold BAL, Hold PC
5	BAH, BAL	Data	Fetch Data	Hold PC
6	2202	Next OP CODE	Fetch Next OP CODE	Finish instruction, Increment PC to 2203

C9.2 Write – 2 Bytes, 5 Cycles

Instruction: STA

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Load OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	IAL	Fetch IAL	Interpret OP CODE, Increment PC to 2202
3	00, IAL	BAL	Fetch BAL	Add 1 to IAL, Hold PC
4	00, IAL+1	BAH	Fetch BAH	Hold BAL, Hold PC
5	BAH, BAL	Data	Write Data	Hold PC
6	2202	Next OP CODE	Fetch Next OP CODE	Increment PC to 2203

C10 INDIRECT,X ADDRESSING

C10.1 Read

Instructions: ADC, AND, CMP, EOR, LDA, ORA, and SBC

Format: XXX (n),X n = Zero page address of absolute address

C10.1a No Page Crossing – 2 Bytes, 5 Cycles

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	IAL	Fetch IAL	Interpret OP CODE, Increment PC to 2202
3	00, IAL	BAL	Fetch BAL	Add 1 to IAL, Hold PC
4	00, IAL+1	BAH	Fetch BAH	Add BAL+X, Hold PC
5	BAH, BAL+X	Data	Fetch Data	Hold PC
6	2202	Next OP CODE	Fetch Next OP CODE	Finish instruction, Increment PC to 2203

C10.1b Page Crossing – 2 Bytes, 6 Cycles

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Load OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	IAL	Fetch IAL	Interpret OP CODE, Increment PC to 2202
3	00, IAL	BAL	Fetch BAL	Add 1 to IAL, Hold PC
4	00, IAL+1	BAH	Fetch BAH	Add BAL to X, Hold PC
5	BAH, BAL+X	Data (Ignored)	Fetch Data (Ignored)	Add BAH+Carry (1), Hold PC
6	BAH+C, BAL+X	Data	Fetch Data	Hold PC
7	2202	Next OP CODE	Fetch Next OP CODE	Finish instruction, Increment PC to 2203

C10.2 Write – 2 Bytes, 6 Cycles

Instruction: STA

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Load OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	IAL	Fetch IAL	Interpret OP CODE, Increment PC to 2202
3	00, IAL	BAL	Fetch BAL	Add 1 to IAL, Hold PC
4	00, IAL+1	BAH	Fetch BAH	Add BAL to X, Hold PC
5	BAH, BAL+X	Data (Ignored)	Fetch Data (Ignored)	Add BAH+Carry (0 or 1) Hold PC
6	BAH+C, BAL+X	Data	Write Data	Hold PC
7	2202	Next OP CODE	Fetch Next OP CODE	Finish instruction, Increment PC to 2203

C11 ACCUMULATOR ADDRESSING

C11.1 1 Byte, 2 Cycles

Instructions: ASL, ASR, LSR, ROL, ROR, and NEG

Format: XXX

Operation: ROL example

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE (ROL)	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	Next OP CODE	Fetch OP CODE (Ignored)	Interpret OP CODE (ROL), Hold PC
3	2201	Next OP CODE	Fetch Next OP CODE	Shift through the Adder, Increment PC to 2202
4	2202	?	Fetch Second Byte	Store result into A, Interpret next OP CODE

C11.2 1 Byte, 3 Cycles

Instruction: LAB

Format: XXX

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	Next OP CODE	Fetch Data (Ignored)	Decode OP CODE, Hold PC
3	2201	Next OP CODE	Fetch Data (Ignored)	
4	2201	Next OP CODE	Fetch Next OP CODE	Increment PC to 2202
5	2202	?	Fetch Second Byte	Store result into A, Interpret next OP CODE

C12 READ/MODIFY/WRITE

C12.1 Zero Page Addressing – 2 Bytes, 5 Cycles

Instructions: ASL, DEC, Increment, LSR, ROL, and ROR

Format: XXX

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE (ROL)	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	ADL	Fetch ADL	Decode OP CODE (ROL), Increment PC to 2202
3	00, ADL	Data	Fetch Data	Hold PC
4	00, ADL	Data	Fetch Data (Ignored)	Perform rotate, Hold PC
5	00, ADL	Shifted Data	Write Data	Set flags, Hold PC
6	2202	OP CODE	Fetch Next OP CODE	Increment PC to 2203

C12.2 Zero Page,X Addressing – 2 Bytes, 6 Cycles

Instructions: ASL, DEC, Increment, LSR, ROL, and ROR

Format: XXX

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE (ROL)	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	BAL	Fetch BAL	Decode OP CODE (ROL), Increment PC to 2202
3	00, BAL	Data (Ignored)	Fetch Data (Ignored)	Add BAH+X, Hold PC
4	00, BAL+X	Data	Fetch Data	Hold PC
5	00, BAL+X	Data	Fetch Data (Ignored)	Perform rotate, Hold PC
6	00, BAL+X	Shifted Data	Write Data	Set flags, Hold PC
7	2202	OP CODE	Fetch Next OP CODE	Increment PC to 2203

C12.3 Absolute Addressing – 3 Bytes, 6 Cycles

Instructions: ASL, DEC, Increment, LSR, ROL, and ROR

Format: XXX nn nn = 2-byte absolute address

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	ADL	Fetch ADL	Decode OP CODE (ROL), Increment PC to 2202
3	2202	ADH	Fetch ADH	Hold ADL, Increment PC to 2203
4	ADH, ADL	Data	Fetch Data	Hold PC
5	ADH, ADL	Data	Fetch Data (Ignored)	Perform rotate, Hold PC
6	ADH, ADL	Shifted Data	Write Data	Set flags, Hold PC
7	2203	OP CODE	Fetch Next OP CODE	Increment PC to 2204

C12.4 Absolute,X Addressing – 3 Bytes, 7 Cycles

Instructions: ASL, DEC, Increment, LSR, ROL, and ROR

Format: XXX nn,X nn = 2-byte absolute address

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE (ROL)	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	BAL	Fetch BAL	Decode OP CODE (ROL), Increment PC to 2202
3	2202	BAH	Fetch BAH	Add BAL+X, Increment PC to 2203
4	BAH, BAL+X	Data (Ignored)	Fetch Data (Ignored)	Add BAH+Carry (0 or 1), Hold PC
5	BAH+C, BAL+X	Data	Fetch Data	Hold PC
6	BAH+C, BAL+X	Data	Fetch Data (Ignored)	Perform rotate, Hold PC
7	BAH+C, BAL+X	Shifted Data	Write Data	Set Flags, Hold PC
8	2203	OP CODE	Fetch Next OP CODE	Increment PC to 2204

C13 BRANCH/JUMP

C13.1 Conditional Branch

Instructions: BCC, BCS, BEQ, BMI, BNE, BPL, BVC, and BVS

Format: XXX r r = 1-byte relative offset

C13.1a Branch Not Taken – 2 Bytes, 2 Cycles

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	Offset	Fetch Offset	Interpret OP CODE, Set previous instruction flags, Increment PC to 2202
3	2202	Next OP CODE	Fetch Next OP CODE	Check flags, Increment PC to 2203

C13.1b Branch Taken with Positive Offset, No Page Boundary Crossing – 2 Bytes, 3 Cycles

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	Offset (+50)	Fetch Offset	Interpret OP CODE, Set previous instruction flags, Increment PC to 2202
3	2202	Next OP CODE	Fetch Next OP CODE	Check flags, Add Offset to PCL, Increment PC to 2203
4	2252	Next OP CODE	Fetch Next OP CODE	Transfer results to PCL, Increment PC to 2253

C13.1c Branch Taken with Negative Offset, Page Boundary Crossed – 2 Bytes, 4 Cycles

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	Offset (–50)	Fetch Offset	Interpret OP CODE, Set previous instruction flags, Increment PC to 2202
3	2202	Next OP CODE	Fetch Next OP CODE	Check flags, Add offset to PCL
4	22B2	Data	Fetch Data (Ignored)	Store Adder result in PCL and subtract 1 from PCH
5	21B2	Next OP CODE	Fetch Next OP CODE	Put out new PCH, Increment PC to 21B3

C13.2 Unconditional Branch Crossing – 2 Bytes, 3 Cycles with Positive Offset, No Page Boundary

Instruction: BRA

Format: XXX r r = 1-byte relative offset

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	Offset (+40)	Fetch Offset	Interpret OP CODE, Increment PC to 2202
3	2202	Next OP CODE	Fetch Next OP CODE	Add offset to PC, Increment PC to 2203
4	2242	Next OP CODE	Fetch Next OP CODE	Increment PC to 2243

C13.3 Jump Absolute – 3 Bytes, 3 Cycles

Instruction: JMP

Format: XXX nn nn = 2-byte absolute address

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	ADL	Fetch ADL	Interpret OP CODE, Increment PC to 2202
3	2202	ADH	Fetch ADH	
4	ADH, ADL	Next OP CODE	Fetch Next OP CODE	ADH, ADL to PC, Increment PC

C13.4 Jump (Indirect,X) – 3 bytes, 6 cycles

Instruction: JMP

Format: XXX (nn,X) nn = 2-byte absolute address

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	IAL	Fetch IAL	Interpret OP CODE, Increment PC to 2202
3	2202	IAH	Fetch IAH	Hold IAL
4	IAH, IAL+X	Data	Fetch Data (Ignored)	Add IAH + carry
5	IAH+C, IAL+X	ADL	Fetch ADL	Add 1 to [IAH, IAL]
6	[IAH+C, IAL+X]+1	ADH	Fetch ADH	
7	ADH, ADL	Next OP CODE	Fetch Next OP CODE	ADH, ADL to PC, Increment PC

C13.5 JMP (Indirect) – 3 Bytes, 5 Cycles

Instruction: JMP

Format: XXX (nn) nn = 2-byte absolute address

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	IAL	Fetch IAL	Interpret OP CODE, Increment PC to 2202
3	2202	IAH	Fetch IAH	Hold IAL
4	IAH, IAL	ADL	Fetch ADL	Add 1 to [IAH, IAL]
5	[IAH, IAL]+1	ADH	Fetch ADH	
6	ADH, ADL	Next OP CODE	Fetch Next OP CODE	ADH, ADL to PC,

C14 STACK

C14.1 Push 1 Byte – 1 byte, 3 Cycles

Instructions: PHA, PHP, PHX, and PHY

Format: XXX

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE (PHA)	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	Next OP CODE	Fetch Next OP CODE (Ignored)	Interpret OP CODE (PHA), Hold PC
3	01FF	(A)	Write A to Stack	Decrement SP to 01FE
4	2201	Next OP CODE	Fetch Next OP CODE	Increment PC to 2203

C14.2 Push 2 Bytes – 1 Byte, 4 Cycles

Instructions: PHI and PHW

Format: XXX

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE (PHI)	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	Next OP CODE	Fetch Next OP CODE (Ignored)	Interpret OP CODE (PHI), Hold PC
3	01FF	(IH)	Write IH to Stack	Decrement SP to 01FE
4	01FE	(IL)	Write IL to Stack	Decrement SP to 01FD
5	2201	Next OP CODE	Fetch Next OP CODE	Increment PC to 2203

C14.3 Push 3 Bytes – 1 Byte, 5 Cycles

Instruction: PSH

Format: XXX

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE (PSH)	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	Next OP CODE	Fetch Next OP CODE (Ignored)	Interpret OP CODE (PSH), Hold PC
3	01FF	(A)	Write A to Stack	Decrement SP to 01FE
4	01FE	(X)	Write X to Stack	Decrement SP to 01FD
5	01FD	(Y)	Write Y to Stack	Decrement SP to 01FC
6	2201	Next OP CODE	Fetch Next OP CODE	Increment PC to 2202

C14.4 Pull 1 Byte – 1 Byte, 4 Cycles

Instructions: PLA, PLP, PLX, and PLY

Format: XXX

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	Next OP CODE	Fetch Next OP CODE and Discard	Interpret OP CODE, Hold PC
3	01FE	Discarded Data	Read Stack	Increment SP to 01FF
4	01FF	Data	Fetch Data	Save Stack
5	2201	Next OP CODE	Fetch Next OP CODE	Data to A

C14.5 Pull 2 Bytes – 1 Byte, 5 Cycles

Instruction: PLW

Format: XXX

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	Next OP CODE	Fetch Next OP CODE and Discard	Interpret OP CODE, Hold PC
3	01FD	Data	Fetch Data (Ignored)	Increment SP to 01FE
4	01FE	WL	Fetch Data from Stack	Increment SP to 01FF
5	01FF	WH	Fetch Data from Stack	Data to WL, Save Stack
6	2201	Next OP CODE	Fetch Next OP CODE	Data to WH

C14.6 Pull 2 Bytes – 1 Byte, 6 Cycles

Instructions: PLI and PIA

Format: XXX

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish Previous Instruction
2	2201	Next OP CODE	Fetch Data (Ignored)	Interpret OP CODE, Hold PC
3	01FD	Data	Fetch Data (Ignored)	Increment SP to 01FE
4	01FE	IL	Fetch Data	Increment SP to 01FF
5	01FF	IH	Fetch Data	Data to IL
6	IH, IL	Data	Fetch Data	Data to IH, Save Stack, Increment I if PIA
7	2201	Next OP CODE	Fetch New OP CODE	Data to A if PIA

C14.7 Pull 3 Bytes – 1 Byte, 6 Cycles

Instructions: PUL

Format: XXX

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE (PUL)	Finish previous instruction, Increment PC to 2201
2	2201	Next OP CODE	Fetch Next OP CODE and Discard	Interpret OP CODE (PUL), Hold PC
3	01FC	Data	Fetch Data (Ignored)	Increment SP to 01FD
4	01FD	Y	Fetch Data from Stack	Increment SP to 01FE
5	01FE	X	Fetch Data from Stack	Data to Y, Increment SP to 01FF
6	01FF	A	Fetch Data from Stack	Data to X
7	2201	Next OP CODE	Fetch Next OP CODE	Data to A

C14.8 Jump to Subroutine – 3 Bytes, 5 Cycles

Instruction: JSR

Format: XXX

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE(JSR)	Finish previous instruction, Increment PC to 2201
2	2201	New ADL	Fetch ADL	Decode OP CODE (JSR), Increment PC to 2202
3	2202	New ADH	Fetch ADH	Hold ADL
4	01FF	PCH	Write PCH to Stack	Hold ADL and ADH, Decrement SP to 01FE
5	01FE	PCL	Write PCL to Stack	Hold ADL and ADH, Decrement SP to 01FD
6	ADH, ADL	New OP CODE	Fetch New OP CODE	ADL to PCL, ADH to PCH

C14.9 Break – 1 Byte, 7 Cycles

Instruction: BRK

Format: XXX

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	Next OP CODE	Fetch Data (Ignored)	Force BRK instruction, Increment PC to 2202
3	01FF	PCH	Store PCH on Stack	Decrement SP to 01FE
4	01FE	PCL	Store PCL on Stack	Decrement SP to 01FD
5	01FD	P	Store P on Stack	Decrement SP to 01FC
6	FFF0	New PCL	Fetch Vector Low	Put Away Stack
7	FFF1	New PCH	Fetch Vector High	Vector Low
8	PCH, PCL	OP CODE	Fetch Interrupt Program	Increment PC to PC + 1

C14.10 Return from Subroutine – 1 Byte, 5 Cycles

Instruction: RTS

Format: XXX

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	3300	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 3301
2	3301	Data	Fetch Data (Ignored)	Decode OP CODE (RTS)
3	3301	Data	Fetch Data (Ignored)	Increment SP to 01FE
4	01FE	PCL (02)	Fetch PCL	Increment SP to 01FF, Hold PCL
5	01FF	PCH (22)	Fetch PCH	
6	2202	Next OP CODE	Fetch Next OP CODE	Increment PC to 2203

C14.11 Return From Interrupt – 1 Byte, 6 Cycles

Instruction: RTI

Format: XXX

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	3300	OP CODE (RTI)	Fetch OP CODE	Finish previous instruction, Increment PC to 3301
2	3301	Data	Fetch Data (Ignored)	Decode OP CODE (RTI)
3	3301	Data	Fetch Data (Ignored)	Increment SP to 01FD
4	01FD	P	Fetch P from Stock	Increment SP to 01FE
5	01FE	PCL (02)	Fetch PCL from Stack	Increment SP to 01FF, Hold PCL
6	01FF	PCH (22)	Fetch PCH from Stack	M to PCL,
Store SP				
7	2202	OP CODE	Fetch OP CODE	Increment New PC

C15 BIT

C15.1 Reset/Set Memory Bit – 2 Bytes, 5 Cycles

Instructions: RMB0 – RMB7, and SMB0 – SMB7

Format: XXX n n = 1-byte zero page address

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	ADL	Fetch ADL	Interpret OP CODE, Increment PC to 2202
3	00, ADL	Data	Fetch Data	Hold PC
4	00, ADL	Data	Fetch Data (Ignored)	Reset (RMB)/set (SMB) bit, Hold PC
5	00, ADL	Modified Data	Write Modified Data	Hold PC
6	2202	Next OP CODE	Fetch Next OP CODE	Finish instruction, Increment PC to 2203

C15.2 Reset/Set Bits in Memory – 4 Bytes, 7 Cycles

Instructions: RBA and SBA

Format: XXX bm,nn bm = 1-byte bit mask, nn = 2-byte absolute address

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	BM	Fetch BM	Interpret OP CODE, Increment PC to 2202
3	2202	ADL	Fetch ADL	Hold BM in Accumulator* Increment PC to 2203
4	2203	ADH	Fetch ADH	Hold ADL, Increment PC to 2204
5	ADH, ADL	Data	Fetch Data	Hold PC
6	ADH, ADL	Data	Fetch Data (Ignored)	Reset(RBA)/Set (SBA) bit, Hold PC
7	ADH, ADL	Modified Data	Write Modified Data	Hold PC
8	2204	Next OP CODE	Fetch Next OP CODE	Finish instruction, Increment PC to 2205

* Note that Accumulator contents are altered by RBA and SBA.

C15.3 Branch on Bit Reset/Set, Branch Not Taken – 3 Bytes, 5 Cycles

Instructions: BBR0 – BBR7, and BBS0 – BBS7

Format: XXX n,r n = 1-byte zero page address, r = offset

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	ADL	Fetch ADL	Interpret OP CODE, Increment PC to 2202
3	00, ADL	Data	Fetch Data	Hold PC
4	00, ADL	Data	Fetch Data (Ignored)	Test the bit, Hold PC
5	2202	Offset	Fetch Branch Offset	Increment PC to 2203
6	2203	Next OP CODE	Fetch Next OP CODE	Finish instruction, Increment PC to 2204

C15.4 Branch on Bit(s) Reset/Set, Branch Not Taken – 5 Bytes, 7 Cycles

Instructions: BAR and BAS

Format: XXX nn, bm, r nn = 2-byte absolute address, bm = 1-byte bit mask,
r = offset

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	ADL	Fetch ADL	Interpret OP CODE, Increment PC to 2202
3	2202	ADH	Fetch ADH	Hold ADL, Increment PC to 2203
4	ADH, ADL	Data	Fetch Data	Hold PC
5	2203	BM	Fetch BM	Hold ADL, ADH Hold PC
6	2203	BM	Fetch BM (Ignored)	Test bits, Increment PC to 2204
7	2204	Offset	Fetch Branch Offset	Increment PC to 2205
8	2205	Next OP CODE	Fetch Next OP CODE	Finish Instruction, Increment PC to 2206

C16 JSB – 1 Byte, 6 Cycles

Instructions: JSB0 – JSB7

Format: XXX

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE (JSB0)	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	Next OP CODE	Fetch Data (Ignored)	Interpret OP CODE (JSB0), Hold PC
3	01FF	PCH	Write PCH to Stack	Decrement SP to 01FE
4	01FE	PCL	Write PCL to Stack	Decrement SP to 01FD
5	FFE0	New PCL	Fetch PCL	Save SP
6	FFE1	New PCH	Fetch PCH	Hold PCL
7	PCH, PCL	First OP CODE	Fetch First OP CODE	Increment PC to PC+1

C17 THREADED CODE

C17.1 INI – 1 Byte, 3 Cycles

Instruction: INI

Format: XXX

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	Next OP CODE	Fetch Data (Ignored)	Interpret OP CODE, Hold PC
3	IH, IL	Data	Fetch Data (Ignored)	Increment I
4	2201	Next OP CODE	Fetch Next OP CODE	Finish instruction, Increment PC to 2202

C17.2 LAI – 1 Byte, 3 Cycles

Instruction: LAI

Format: XXX

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	Next OP CODE	Fetch Data (Ignored)	Interpret OP CODE, Hold PC
3	IH, IL	Data	Fetch Data	
4	2201	Next OP CODE	Fetch Next OP CODE	Data to A, Increment PC to 2202

C17.3 LAN – 1 Byte, 3 Cycles

Instruction: LAN

Format: XXX

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	Next OP CODE	Fetch Data (Ignored)	Interpret OP CODE, Hold PC
3	IH, IL	Data	Fetch Data	Increment I
4	2201	Next OP CODE	Fetch Next OP CODE	Finish instruction, Data to A Increment PC to 2202

C17.4 NXT – 1 Byte, 4 Cycles

Instruction: NXT

Format: XXX

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	Next OP CODE	Fetch Data (Ignored)	Interpret OP CODE
3	IH, IL	New PCL	Fetch New PCL	
4	[IH, IL] + 1	New PCH	Fetch New PCH	Hold PCL
5	PCH, PCL	Next OP CODE	Fetch New OP CODE	Finish instruction, Increment PC to PC + 1

C17.5 LII – 1 Byte, 5 Cycles

Instruction: LII

Format: XXX

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	Next OP CODE	Ignore	Interpret OP CODE, Hold PC
3	IH, IL	New IL	Fetch IL	
4	[IH, IL] + 1	New IH	Fetch IH	Hold IL
5	New IH, IL	Data	Fetch Data (Ignored)	New IH, IL → I
6	2201	Next OP CODE	Fetch New OP CODE	Increment PC to 2202

C17.6 JPI – 3 Bytes, 5 Cycles

Instruction: JPI

Format: XXX

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Increment PC to 2201
2	2201	IAL	Fetch IAL	Interpret OP CODE, Increment PC to 2202
3	2202	IAH	Fetch IAH	Save IAL,
4	IAH, IAL	ADL	Fetch ADL	[IAH, IAL] + 1
5	[IAH, IAL] + 1	ADH	Fetch ADH	Save ADL
6	ADH, ADL	Next OP CODE	Fetch New OP CODE	Finish instruction, Increment PC to [ADH, ADL] + 1

C18 START AND INTERRUPT SEQUENCES

C18.1 Start Sequence (Power-On)

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	?	?	Fetch Data (Ignored)	Hold During Reset
2	? + 1	?	Fetch Data (Ignored)	First Start State
3	01, SP	?	Fetch Data (Ignored)	Second Start State
4	01, SP–1	?	Fetch Data (Ignored)	Third Start State
5	01, SP–2	?	Fetch Data (Ignored)	Fourth Start State
6	FFFE	PCL	Fetch PCL	
7	FFFF	PCH	Fetch PCH	Hold PCL
8	PCH, PCL	First OP CODE	Fetch First OP CODE	Increment PC to [PCH, PCL] + 1

C18.2 Interrupt Sequence (NMI) *

Operation:

Cycle	Address Bus	Data Bus	Bus Operation	CPU Operation
1	2200	OP CODE	Fetch OP CODE	Finish previous instruction, Hold PC
2	2200	OP CODE	Fetch OP CODE	Force a BRK Instruction, Hold PC
3	01FF	PCH	Store PCH on Stack	Decrement SP to 01FE
4	01FE	PCL	Store PCL on Stack	Decrement SP to 01FD
5	01FD	P	Store P on Stack	Decrement SP to 01FC
6	FFFC	PCL	Fetch PCL	
7	FFFD	PCH	Fetch PCH	Hold PCL
8	PCH, PCL	Next OP CODE	Fetch Interrupt Program First OP CODE	Increment PC to PC + 1

* All other interrupts are identical except for different vector locations at cycles 6 and 7.